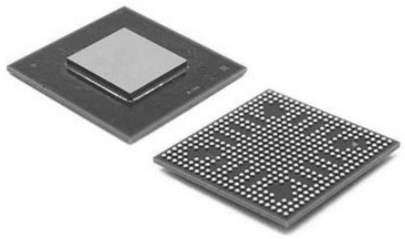
ADM1272-1ACPZ-RL

Data Sheet

High Voltage Positive Hot Swap Controller and Digital Power Monitor with PMBus

Manufacturers	Analog Devices, Inc
Package/Case	48-Lead LFCSP (8mm x 7mm w/ EP)
Product Type	Power Supplies
RoHS	
Lifecycle	



Images are for reference only

Please submit RFQ for ADM1272-1ACPZ-RL or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The ADM1272 is a hot swap controller that allows a circuit board to be removed from or inserted into a live backplane. It also features current, voltage, and power readback via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus™ interface. This device is able to withstand up to 120 V, which makes it very robust in surviving surges and transients commonly associated with high voltage systems, usually clamped using protection devices such as transient voltage suppressors (TVSs) that can often exceed 100 V.

The load current, ILOAD, is measured using an internal current sense amplifier that measures the voltage across a sense resistor in the power path via the SENSE+ and SENSE− pins. A default current limit sense voltage of 30 mV is set, but this limit can be adjusted down, if required, using a resistor divider network from the VCAP regulator output voltage to the ISET pin. An additional resistor can also be placed from ISET to VIN (or VOUT) to allow the current limit to track inversely with the rail voltage. This resistor allows an approximate system power limit to be used.

The ADM1272 limits the current through the sense resistor by controlling the gate voltage of an external N channel field effect transistor (FET) in the power path. The sense voltage, and therefore the load current, is maintained below the preset maximum. The ADM1272 protects the external FET by monitoring and limiting the energy transfer through the FET while the current is being controlled. This energy limit is set by the choice of components connected to the EFAULT pin (for fault protection mode) and the ESTART pin during startup. Therefore, different energy limits can be set for start-up and normal fault conditions. During startup, inrush currents are maintained very low and different areas of the safe operating area (SOA) curve are of interest, whereas during fault conditions, the currents can be much higher.

The controller uses the drain to source voltage (VDS) across the FET to set the current profile of the EFAULT and ESTART pins and, therefore, the amount of much energy allowed to be transferred in the FET. This energy limit ensures the MOSFET remains within the SOA limits. Optionally, use a capacitor on the DVDT pin to set the output voltage ramp rate, if required. In case of a short-circuit event, a fast internal overcurrent detector responds in hundreds of ns and signals the gate to shut down. A 1.5 A pull-down device ensures a fast FET response. The gate then recovers control within 50 µs to ensure minimal disruption during conditions, such as line steps and surges. The ADM1272 features overvoltage (OV) and undervoltage (UV) protection, programmed using external resistor dividers on the UVH, UVL, and OV pins. The use of two pins for undervoltage allows independent accurate rising and falling thresholds. The PWRGD output pin signals when the output voltage is valid and the gate is sufficiently enhanced. The validity of VOUT is determined using the PWGIN pin.

The 12-bit ADC measures the voltage across the sense resistor, the supply voltage on the SENSE+ pin, the output voltage, and the temperature using an external NPN/PNP device. A PMBus interface allows a controller to read data from the ADC. As many as 16 unique I2C addresses can be selected, depending on how the two ADRx pins are connected. The ADM1272 is available in a custom 48-lead LFCSP (7 mm × 8 mm) with a pinstrap mode that allows the device to be configured for automatic retry or latchoff when an overcurrent (OC) fault occurs.

Features

Controls supply voltages from 16 V to 80 V (absolute maximum 120 V)

High voltage (80 V) IPC-9592 compliant packaging

FET energy monitoring for adaptable FET SOA protection

Gate boost mode for fast recovery from OC transients

Programmable random start mode to stagger power-on

FET fault detection

Remote temperature sensing with programmable warning and shutdown thresholds

Programmable 2.5 mV to 30 mV system current-limit setting range

ILOAD, VIN, VOUT, temperature, power, and energy telemetry

Programmable start-up current limit

Programmable linear output voltage soft start

1% accurate UV and OV thresholds

Programmable hot swap restart function

2 programmable GPIO pins

Reports power and energy consumption

Peak detect registers for current, voltage, and power

PMBus fast mode compliant interface

48-lead 7 mm × 8 mm LFCSP

Application

48 V/54 V systems

Servers

Power monitoring and control/power budgeting

Central office equipment

Telecommunication and data communication equipment

Industrial applications

Related Products

ADV7123KST140

Analog Devices, Inc

QFP-48

ADUM7223ACCZ

Analog Devices, Inc

LGA-13

ADUM3223CRZ

Analog Devices, Inc

SOIC-16

ADUM1234BRWZ

Analog Devices, Inc

SOIC-16

[ADV7171KSU]

Analog Devices, Inc

TQFP44

[AD6645ASQZ-80]

Analog Devices, Inc

QFP52

[AD6645ASQZ-105]

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