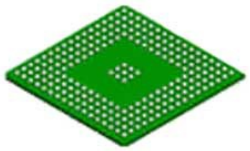
AD9249BBCZ-65

Data Sheet

Analogue to Digital Converter, 14 bit, 65 MSPS, Differential, Single Ended, SPI, Single, 1.7 V

Manufacturers	Analog Devices, Inc
Package/Case	IC ADC 14BIT 65MSPS 144CSPBGA
Product Type	Data Conversion ICs
RoHS	Pb-free Halide free
Lifecycle	



Images are for reference only

Please submit RFQ for AD9249BBCZ-65 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The ADC requires a single 1.8 V power supply and an LVPECL-/ CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The AD9249 automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. Data clock outputs (DCO±1, DCO±2) for capturing data on the output and frame clock outputs (FCO±1, FCO±2) for signaling a new output byte are provided. Individual channel power-down is supported, and the device typically consumes less than 2 mW when all channels are disabled.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation.

The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9249 is available in an RoHS-compliant, 144-ball CSP-BGA. It is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

Small Footprint. Sixteen ADCs are contained in a small, 10 mm × 10 mm package.

Low Power of 35 mW/Channel at 20 MSPS with scalable power options.

Ease of Use. Data clock outputs (DCO±1, DCO±2) operate at frequencies of up to 455 MHz and support double data rate (DDR) operation.

User Flexibility. SPI control offers a wide range of flexible features to meet specific system requirements.

Features

Low power16 ADC channels integrated into 1 package58 mW per channel at 65 MSPS with scalable power options35 mW per channel at 20 MSPS

SNR: 75 dBFS (to Nyquist); SFDR: 90 dBc (to Nyquist)

DNL: ±0.6 LSB (typical); INL: ±0.9 LSB (typical)

Crosstalk, worst adjacent channel, 10 MHz, −1 dBFS:−90 dB typical

Serial LVDS (ANSI-644, default)Low power, reduced signal option (similar to IEEE 1596.3)

Data and frame clock outputs

650 MHz full power analog bandwidth

2 V p-p input voltage range

1.8 V supply operation

See datasheet for additional features

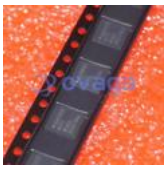
Application

Medical imaging

Communications receivers

Multichannel data acquisition

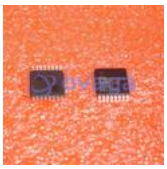
Related Products



ADAS3022BCPZ

Analog Devices, Inc

LFCSP-40



AD7266BSUZ

Analog Devices, Inc

TQPF-32

AD574AJNZ

Analog Devices, Inc

PDIP-28

AD7401YRWZ

Analog Devices, Inc

SOIC-16

AD7938BSUZ

Analog Devices, Inc

TQFP-32

AD7192BRUZ-REEL

Analog Devices, Inc

TSSOP-24

AD7124-8BCPZ-RL7

Analog Devices, Inc

LFCSP-32

AD9680BCPZ-500

Analog Devices, Inc

LFCSP-64