Fanout Buffer, 1.2 GHz, 12 LVDS / 24 CMOS Outputs, 1.71 V to 1.89 V supply, LFCSP-48

Manufacturers	Analog Devices, Inc
Package/Case	LFCSP-48
Product Type	Clock & Timer ICs
RoHS	Rohs
Lifecycle	

FUNCTIONAL BLOCK DIAGRAM

Figure 1.
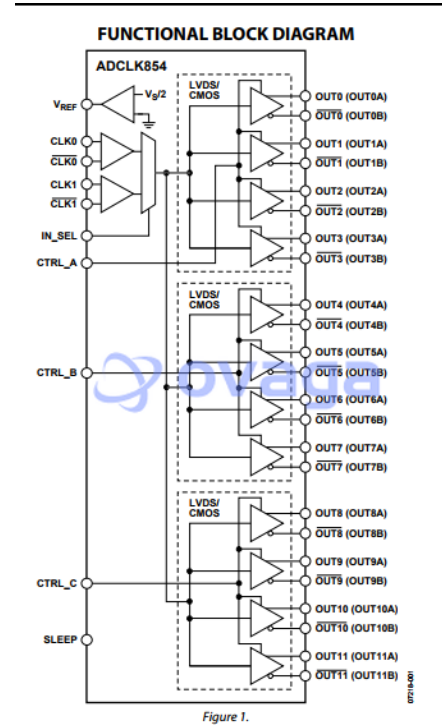
Images are for reference only

Please submit RFQ for ADCLK854BCPZ or Email to us: sales@ovaga.com We will contact you in 12 hours.　　RFQ

General Description

The ADCLK854 offers two selectable inputs and a sleep mode feature. The IN_SEL pin state determines which input is fanned out to all the outputs. The SLEEP pin enables a sleep mode to power down the device.

The inputs accept various types of single-ended and differential logic levels including LVPECL, LVDS, HSTL, CML, and CMOS. Table 8 provides interface options for each type of connection.

This device is available in a 48-pin LFCSP package. It is specified for operation over the standard industrial temperature range of −40°C to +85°C.

Features

2 selectable differential inputs

Selectable LVDS/CMOS outputs

Up to 12 LVDS (1.2 GHz) or 24 CMOS (250 MHz) outputs

54 fs rms integrated jitter (12 kHz to 20 MHz)

100 fs rms additive broadband jitter

2.0 ns propagation delay (LVDS)

135 ps output rise/fall (LVDS)

70 ps output-to-output skew (LVDS)

Sleep mode

Pin programmable control

1.8 V power supply

Application

Low jitter clock distribution

Clock and data signal restoration

Level translation

Wireless communications

Wired communications

Medical and industrial imaging

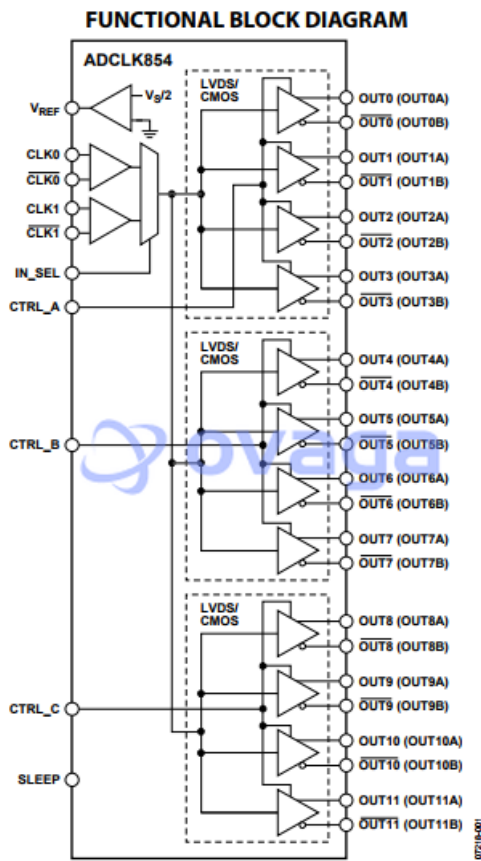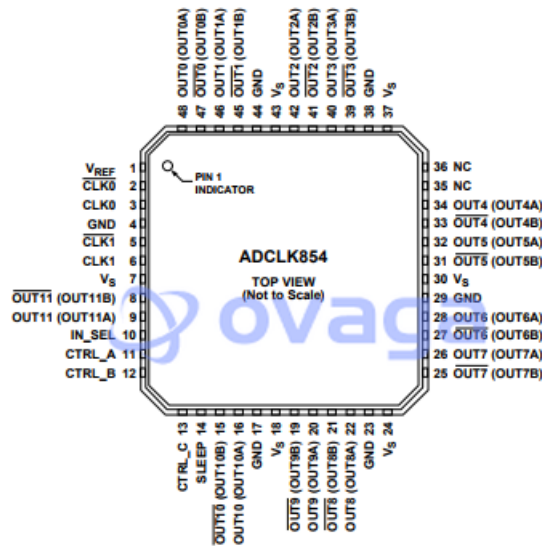ATE and high performance instrumentation

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

NOTES:
1. NC = NO CONNECT.
2. EXPOSED PADDLE MUST BE CONNECTED TO GND.

Figure 2. Pin Configuration

Related Products

ADF4350BCPZ

Analog Devices, Inc

LFCSP-32

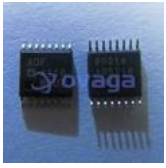**AD9516-4BCPZ**

Analog Devices, Inc

LFCSP64

ADF4111BRUZ

Analog Devices, Inc

TSSOP-16

ADF4113BRUZ

Analog Devices, Inc

TSSOP-16

ADF4116BRUZ

Analog Devices, Inc

TSSOP-16

ADF4110BRUZ

Analog Devices, Inc

TSSOP-16

ADF4193BCPZ

Analog Devices, Inc

LFCSP-32

AD2S99BPZ

Analog Devices, Inc

PLCC-20