

# X9271UV14IZ-2.7

Data Sheet

Single Digitally-Controlled (XDCP<sup>TM</sup>) Potentiometer; Temperature Range: -40°C to 85°C; Package: 14-TSSOP

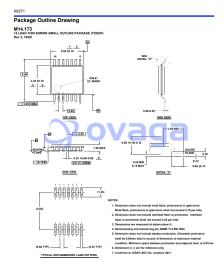
Manufacturers Renesas Technology Corp

Package/Case TSSOP-14

Product Type Logic ICs

RoHS

Lifecycle



Images are for reference only

Please submit RFQ for X9271UV14IZ-2.7 or <a href="mailto:sales@ovaga.com"><u>Emailto:sales@ovaga.com</u></a> We will contact you in 12 hours.

**RFQ** 

## **General Description**

The X9271 integrates a single, digitally controlled potentiometer (XDCP<sup>TM</sup>) on a monolithic CMOS integrated circuit. The digitally controlled potentiometer is implemented by using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four nonvolatile data registers that can be directly written to and read by the user. The contents of the WCR control the position of the wiper on the resistor array though the switches. Power-up recalls the contents of the default data register (DR0) to the WCR. The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

# **Features**

256 Resistor Taps

SPI Serial Interface for Write, Read, and Transfer Operations of Potentiometer

Wiper Resistance, 100Ω typical at>

16 Nonvolatile Data Registers

Nonvolatile Storage of Multiple Wiper Positions

Power-on Recall; Loads Saved Wiper Position on Power-up

Standby Current  $<3\mu A$  Max

 $50k\Omega$  End-to-End Resistance

100-yr Data Retention

Endurance: 100,000 Data Changes per Bit per Register

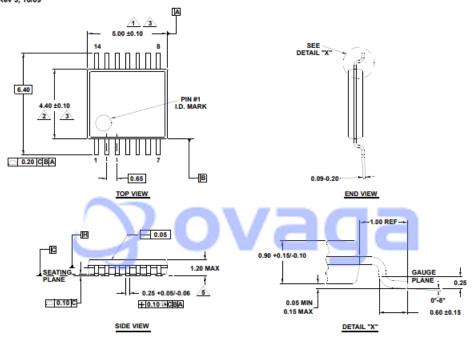
14-Lead TSSOP

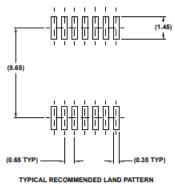
Low-power CMOS

Pb-Free Plus Anneal Available (RoHS Compliant)

### **Package Outline Drawing**

M14.173
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 3, 10/09





#### NOTES:

- ion does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
- 2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
- ensions are measured at datum plane H.
- 4. Dimensioning and tolerancing per ASME Y14.5M-1994.
- ension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
- 6. Dimension in ( ) are for reference only.
- 7. Conforms to JEDEC MO-153, variation AB-1.

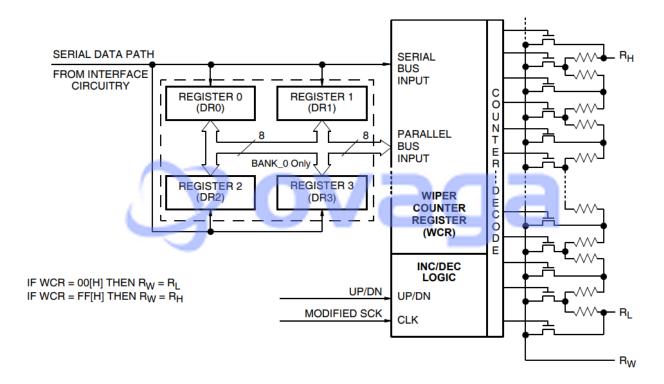


FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

#### **Related Products**

