# AD9255BCPZ-80

Data Sheet

1-Channel Single ADC Pipelined 80Msps 14-bit Parallel/Serial (3-Wire, SPI)/LVDS 48-Pin LFCSP EP Tray

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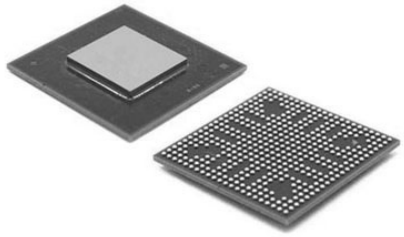
|---|---|
| Manufacturers | Analog Devices, Inc |
| Package/Case | LFCSP-48 |
| Product Type | Data Conversion ICs |
| RoHS | Rohs |
| Lifecycle | |



Images are for reference only

Please submit RFQ for AD9255BCPZ-80 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

## General Description

The AD9255 is a 14-bit, 125 MSPS analog-to-digital converter (ADC). The AD9255 is designed to support communications applications where high performance combined with low cost, small size, and versatility is desired.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic to provide 14-bit accuracy at 125 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The ADC features a wide bandwidth differential sample-and-hold analog input amplifier supporting a variety of user-selectable input ranges. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available ADCs, the AD9255 is suitable for applications in communications, instrumentation, and medical imaging.

A differential clock input controls all internal conversion cycles. A duty cycle stabilizer provides the means to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance over a wide range of input clock duty cycles. An integrated voltage reference eases design considerations.

The ADC output data format is either parallel 1.8 V CMOS or LVDS (DDR). A data output clock is provided to ensure proper latch timing with receiving logic.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface. Flexible power-down options allow significant power savings, when desired. An optional on-chip dither function is available to improve SFDR performance with low power analog input signals.

The AD9255 is available in a Pb-free, 48-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

**Applications**

On-chip dither option for improved SFDR performance with low power analog input.

Proprietary differential input that maintains excellent SNR performance for input frequencies up to 300 MHz.

Operation from a single 1.8 V supply and a separate digital output driver supply accommodating 1.8 V CMOS or LVDS outputs

Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, test modes, and voltage reference mode.

Pin compatibility with the AD9265, allowing a simple migration up to 16 bits.

## Features

Low power: 371 mW @ 125 MSPS

1.8 V analog supply operation

1.8 V CMOS or LVDS output supply

Integer 1-to-8 input clock divider

IF sampling frequencies to 300 MHz

Optional on-chip dither

Programmable internal ADC voltage reference

Integrated ADC sample-and-hold inputs

See data sheet for additional features

## Application

Communications

Multimode digital receivers (3G)

GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, and TD-SCDMA

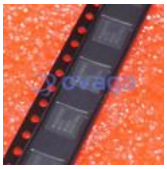
Smart antenna systems

General-purpose software radios

Broadband data applications

Ultrasound equipment

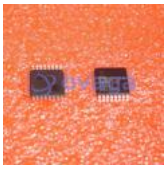
### Related Products



ADAS3022BCPZ

Analog Devices, Inc

LFCSP-40



AD7266BSUZ

Analog Devices, Inc

TQPF-32

AD574AJNZ

Analog Devices, Inc

PDIP-28

AD7401YRWZ

Analog Devices, Inc

SOIC-16

AD7938BSUZ

Analog Devices, Inc

TQFP-32

AD7192BRUZ-REEL

Analog Devices, Inc

TSSOP-24

AD7124-8BCPZ-RL7

Analog Devices, Inc

LFCSP-32

AD9680BCPZ-500

Analog Devices, Inc

LFCSP-64